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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/810,941	03/16/2001	Hrvoje Bilic	6727/1G912US1	7239

7278 7590 12/07/2004

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EXAMINER	
YAO, KWANG BIN	

ART UNIT	PAPER NUMBER
2667	

DATE MAILED: 12/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/810,941	BILIC ET AL.	
	Examiner	Art Unit	
	Kwang B. Yao	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/20/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1- 3, 9-11, 13, 14, 16-18, 27-32, 38, 40-42, 52 are rejected under 35 U.S.C. 102(b) as being anticipated by Bremer et al. (US 6,032,190).

Bremer et al. discloses a communication system comprising the following features: regarding claim 1, a network interface device, comprising: host interface logic (Fig. 3, Switch Fabric out 60, Switch Fabric In 62), arranged to receive from a host processor (Fig. 2, Switch Fabric 38, Media Card 20) a frame of outgoing data that includes outgoing header information and outgoing payload data, and to separate the header information from the payload data; an outgoing data memory (Fig. 3, Data 66), coupled to receive the outgoing payload data from the host interface logic (Fig. 3, Switch Fabric out 60, Switch Fabric In 62); an outgoing header memory (Fig. 3, Header 64), coupled to receive the outgoing header information from the host interface logic (Fig. 3, Switch Fabric out 60, Switch Fabric In 62); a transmit protocol processor (Fig. 3, PPU 68), coupled to read and process the outgoing header information from the outgoing header memory (Fig. 3, Header 64) so as to generate at least one outgoing packet header in accordance with a predetermined network protocol; and transmit logic (Fig. 3, DMA 63, Queues 72), coupled to receive and associate the at least one outgoing packet header

with the outgoing payload data from the outgoing data memory (Fig. 3, Data 66), so as to generate at least one outgoing data packet for transmission over a network in accordance with the protocol; regarding claim 2, wherein the protocol comprises a network layer protocol (column 1, lines 11-13; column 8, lines 5-8); regarding claim 3, wherein the network layer protocol (column 1, lines 11-13; column 8, lines 5-8) comprises an Internet Protocol IP (column 1, lines 11-13; column 8, lines 5-8); regarding claim 9, wherein the outgoing header memory (Fig. 3, Header 64) comprises a fast memory, coupled to the transmit protocol processor (Fig. 3, PPU 68) so as to be accessed thereby in a single clock cycle (column 12, lines 21-24) of the processor; regarding claim 10, wherein at least the outgoing data and header memories and the transmit logic (Fig. 3, DMA 63, Queues 72) are contained together with the transmit protocol processor (Fig. 3, PPU 68) in a single integrated circuit chip, and wherein the transmit protocol processor (Fig. 3, PPU 68) is coupled to the host interface logic (Fig. 3, Switch Fabric out 60, Switch Fabric In 62) so as to enable reprogramming of the transmit protocol processor (Fig. 3, PPU 68); regarding claim 11, wherein the at least one outgoing packet header comprises a plurality of outgoing packet headers, and wherein the transmit logic (Fig. 3, DMA 63, Queues 72) is arranged to associate each of the outgoing packet headers with a corresponding portion of the outgoing payload data so as to generate a sequence of outgoing data packets; regarding claim 13, receive logic (Fig. 3, Ingress 40, Box 44), which is coupled to receive from the network an incoming data packet comprising incoming data that includes an incoming header and incoming payload data, and to select a header portion of the incoming data packet; an incoming header memory (Fig. 3, Header 48), coupled to receive from the receive logic (Fig. 3, Ingress 40, Box 44) a header portion of the

incoming data, which includes at least the incoming header; an incoming data memory (Fig. 3, Data 50), coupled to receive from the receive logic (Fig. 3, Ingress 40, Box 44) a data portion of the incoming data, which includes at least the incoming payload data; and a receive protocol processor (Fig. 3, PPU 54), coupled to read and process the header portion of the incoming data in accordance with the predetermined network protocol so as to generate incoming header information, wherein the host interface logic (Fig. 3, Switch Fabric out 60, Switch Fabric In 62) is coupled to receive and associate the incoming header information with the incoming payload data so as to generate an incoming data frame for delivery to the host processor (Fig. 2, Switch Fabric 38, Media Card 20); regarding claim 14, wherein the transmit protocol processor (Fig. 3, PPU 68) and the receive protocol processor (Fig. 3, PPU 54) are contained together in a single integrated circuit chip, and comprising a bus on the chip coupled to both the transmit and receive protocol processor (Fig. 3, PPU 54)s; regarding claim 16, a network interface device, comprising: receive logic (Fig. 3, Ingress 40, Box 44), which is coupled to receive from a network in accordance with a predetermined network protocol an incoming data packet comprising incoming data that includes an incoming header and incoming payload data, and which is arranged to select a header portion of the incoming data packet; an incoming header memory (Fig. 3, Header 48), coupled to receive from the receive logic (Fig. 3, Ingress 40, Box 44) a header portion of the incoming data, which includes at least the incoming header; an incoming data memory (Fig. 3, Data 50), coupled to receive from the receive logic (Fig. 3, Ingress 40, Box 44) a data portion of the incoming data, which includes at least the incoming payload data; a receive protocol processor (Fig. 3, PPU 54), coupled to read and process the header portion of the

incoming data in accordance with the predetermined network protocol so as to generate incoming header information; and host interface logic (Fig. 3, Switch Fabric out 60, Switch Fabric In 62), which is coupled to receive and associate the incoming header information with the incoming payload data so as to generate an incoming data frame for delivery to a host processor (Fig. 2, Switch Fabric 38, Media Card 20); regarding claim 17, wherein the protocol comprises a network layer protocol (column 1, lines 11-13; column 8, lines 5-8); regarding claim 18, wherein the network layer protocol (column 1, lines 11-13; column 8, lines 5-8) comprises an Internet Protocol IP (column 1, lines 11-13; column 8, lines 5-8); regarding claim 27, wherein the outgoing header memory (Fig. 3, Header 64) comprises a fast memory, coupled to the receive protocol processor (Fig. 3, PPU 54) so as to be accessed thereby in a single clock cycle (column 12, lines 21-24) of the processor; regarding claim 28, wherein at least the incoming data and header memories and the receive logic (Fig. 3, Ingress 40, Box 44) are contained together with the receive protocol processor (Fig. 3, PPU 54) in a single integrated circuit chip, and wherein the receive protocol processor (Fig. 3, PPU 54) is coupled to the host interface logic (Fig. 3, Switch Fabric out 60, Switch Fabric In 62) so as to enable reprogramming of the receive protocol processor (Fig. 3, PPU 54); regarding claim 29, wherein the host interface logic (Fig. 3, Switch Fabric out 60, Switch Fabric In 62) comprises a direct memory access DMA engine, and wherein the receive protocol processor (Fig. 3, PPU 54) is arranged to generate DMA descriptor (column 5, lines 33-37)s along with the incoming header information, so that the DMA engine writes the incoming data frame to a memory of the host processor (Fig. 2, Switch Fabric 38, Media Card 20) responsive to the descriptor (column 5, lines 33-37)s; regarding claim 30, a method for transmitting

data over a packet network, comprising: receiving from a host processor (Fig. 2, Switch Fabric 38, Media Card 20) a frame of outgoing data that includes outgoing header information and outgoing payload data; writing the outgoing header information to an outgoing header memory (Fig. 3, Header 64); writing the outgoing payload data to an outgoing payload memory, separate from the header memory; reading and processing the outgoing header information from the outgoing header memory (Fig. 3, Header 64) so as to generate at least one outgoing packet header in accordance with a predetermined network protocol; and associating the at least one outgoing packet header with the outgoing payload data from the outgoing data memory (Fig. 3, Data 66), so as to generate at least one outgoing data packet for transmission over the network in accordance with the protocol; regarding claim 31, wherein the protocol comprises a network layer protocol (column 1, lines 11-13; column 8, lines 5-8); regarding claim 32, wherein the network layer protocol (column 1, lines 11-13; column 8, lines 5-8) comprises an Internet Protocol IP (column 1, lines 11-13; column 8, lines 5-8); regarding claim 38, wherein processing the outgoing header information comprises generating a plurality of outgoing packet headers, and wherein associating the at least one outgoing packet header with the outgoing payload data comprises associating each of the plurality of outgoing packet headers with a corresponding portion of the outgoing payload data so as to generate a sequence of outgoing data packets; regarding claim 40, a method for processing data received over a packet network, comprising: receiving from a network in accordance with a predetermined network protocol an incoming data packet comprising incoming data that includes an incoming header and incoming payload data; writing a header portion of the incoming data packet to an incoming header memory (Fig. 3, Header 48), the header

portion including at least the incoming header; writing a data portion of the incoming data to an incoming data memory (Fig. 3, Data 50), separate from the incoming header memory (Fig. 3, Header 48), the data portion including at least the incoming payload data; reading and processing the header portion of the incoming data from the incoming header memory (Fig. 3, Header 48) in accordance with the predetermined network protocol so as to generate incoming header information; and associating the incoming header information with the incoming payload data from the incoming data memory (Fig. 3, Data 50) so as to generate an incoming data frame for delivery to a host processor (Fig. 2, Switch Fabric 38, Media Card 20); regarding claim 41, wherein the protocol comprises a network layer protocol (column 1, lines 11-13; column 8, lines 5-8); regarding claim 42, wherein the network layer protocol (column 1, lines 11-13; column 8, lines 5-8) comprises an Internet Protocol IP (column 1, lines 11-13; column 8, lines 5-8); regarding claim 52, wherein processing the header portion comprises generating a direct memory access DMA descriptor (column 5, lines 33-37), and comprising writing the incoming data frame to a memory of the host processor (Fig. 2, Switch Fabric 38, Media Card 20) responsive to the descriptor (column 5, lines 33-37). See column 3-12.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4-6, 12, 19-21, 25, 26, 33-35, 39, 43-45, 49-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bremer et al. (US 6,032,190) in view of Narisi et al. (US 6,810,431).

Bremer et al. discloses the claimed limitations above. Bremer et al. does not disclose the following features: regarding claim 4, wherein the protocol comprises a transport layer protocol; regarding claim 5, wherein the transport layer protocol comprises a Transport Control Protocol TCP; regarding claim 6, wherein the transport layer protocol comprises a User Datagram Protocol UDP; regarding claim 12, wherein the at least one outgoing packet header comprises a data length parameter, and wherein the transmit logic is arranged to read the data for inclusion in the outgoing packet responsive to the data length parameter; regarding claim 19, wherein the protocol comprises a transport layer protocol; regarding claim 20, wherein the transport layer protocol comprises a Transport Control Protocol TCP; regarding claim 21, wherein the transport layer protocol comprises a User Datagram Protocol UDP; regarding claim 25, wherein the data portion of the incoming data comprises substantially all of the incoming data, and wherein the header information comprises an instruction to the host interface logic, indicating a length of the payload data to read from the data portion in the data memory for inclusion in the incoming data frame; regarding claim 26, wherein the receive logic comprises a control register, which is programmable with a length parameter, responsive to which the receive logic determines how many bits to select for inclusion in the header portion; regarding claim 33, wherein the protocol comprises a transport layer protocol; regarding claim 34, wherein the transport layer protocol comprises a Transport Control Protocol TCP; regarding claim 35, wherein the transport

layer protocol comprises a User Datagram Protocol UDP; regarding claim 39, wherein processing the outgoing header information comprises determining a data length parameter, and wherein associating the at least one outgoing packet header with the outgoing payload data comprises reading the data from the outgoing payload memory for inclusion in the outgoing packet responsive to the data length parameter; regarding claim 43, wherein the protocol comprises a transport layer protocol; regarding claim 44, wherein the transport layer protocol comprises a Transport Control Protocol TCP; regarding claim 45, wherein the transport layer protocol comprises a User Datagram Protocol UDP; regarding claim 49, wherein writing the data portion of the incoming data comprises writing substantially all of the incoming data to the incoming data memory, and wherein processing the header portion comprises writing an instruction indicating a length of the payload data to read from the data portion in the data memory for inclusion in the incoming data frame; regarding claim 50, wherein writing the header portion comprises programming a control register with a length parameter, and determining how many bits to select for inclusion in the header portion responsive to the length parameter; regarding claim 51, wherein programming the control register comprises determining the length parameter based on a maximum header length permitted by the network protocol.

Narisi et al. discloses a communication system comprising the following features: regarding claim 4, wherein the protocol comprises a transport layer protocol (column 14, lines 47-54); regarding claim 5, wherein the transport layer protocol (column 14, lines 47-54) comprises a Transport Control Protocol TCP (column 14, lines 47-54); regarding claim 6, wherein the transport layer protocol (column 14, lines 47-54) comprises a User Datagram Protocol UDP (column 14, lines 47-54); regarding claim 12, wherein the at

least one outgoing packet header comprises a data length (column 29, lines 50-63) parameter, and wherein the transmit logic is arranged to read the data for inclusion in the outgoing packet responsive to the data length (column 29, lines 50-63) parameter; regarding claim 19, wherein the protocol comprises a transport layer protocol (column 14, lines 47-54); regarding claim 20, wherein the transport layer protocol (column 14, lines 47-54) comprises a Transport Control Protocol TCP (column 14, lines 47-54); regarding claim 21, wherein the transport layer protocol (column 14, lines 47-54) comprises a User Datagram Protocol UDP (column 14, lines 47-54); regarding claim 25, wherein the data portion of the incoming data comprises substantially all of the incoming data, and wherein the header information comprises an instruction to the host interface logic, indicating a length (column 29, lines 50-63) of the payload data to read from the data portion in the data memory for inclusion in the incoming data frame; regarding claim 26, wherein the receive logic comprises a control register, which is programmable with a length (column 29, lines 50-63) parameter, responsive to which the receive logic determines how many bits to select for inclusion in the header portion; regarding claim 33, wherein the protocol comprises a transport layer protocol (column 14, lines 47-54); regarding claim 34, wherein the transport layer protocol (column 14, lines 47-54) comprises a Transport Control Protocol TCP (column 14, lines 47-54); regarding claim 35, wherein the transport layer protocol (column 14, lines 47-54) comprises a User Datagram Protocol UDP (column 14, lines 47-54); regarding claim 39, wherein processing the outgoing header information comprises determining a data length (column 29, lines 50-63) parameter, and wherein associating the at least one outgoing packet header with the outgoing payload data comprises reading the data from the outgoing

payload memory for inclusion in the outgoing packet responsive to the data length (column 29, lines 50-63) parameter; regarding claim 43, wherein the protocol comprises a transport layer protocol (column 14, lines 47-54); regarding claim 44, wherein the transport layer protocol (column 14, lines 47-54) comprises a Transport Control Protocol TCP (column 14, lines 47-54); regarding claim 45, wherein the transport layer protocol (column 14, lines 47-54) comprises a User Datagram Protocol UDP (column 14, lines 47-54); regarding claim 49, wherein writing the data portion of the incoming data comprises writing substantially all of the incoming data to the incoming data memory, and wherein processing the header portion comprises writing an instruction indicating a length (column 29, lines 50-63) of the payload data to read from the data portion in the data memory for inclusion in the incoming data frame; regarding claim 50, wherein writing the header portion comprises programming a control register with a length (column 29, lines 50-63) parameter, and determining how many bits to select for inclusion in the header portion responsive to the length (column 29, lines 50-63) parameter; regarding claim 51, wherein programming the control register comprises determining the length (column 29, lines 50-63) parameter based on a maximum header length (column 23, lines 1-15) permitted by the network protocol. It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Bremer et al., by using the features, as taught by Narisi et al., in order to provide less costly development and optimize network performance. See Narisi et al., column 10, line 58 to column 11, line 4.

5. Claims 7, 8, 22, 23, 36, 37, 46-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bremer et al. (US 6,032,190) in view of Denton et al. (US 6,041,043).

Bremer et al. discloses the claimed limitations above. Moreover, Bremer et al. discloses the following features: regarding claim 7, wherein the outgoing header memory comprise parallel first-in-first-out FIFO buffers (Fig. 5, Input FIFO 182, Output FIFO 184), which are arranged to hold the outgoing payload data and outgoing header information, respectively, for a plurality of frames of outgoing data; regarding claim 8, wherein the outgoing header memory comprises a first FIFO buffer (Fig. 5, Input FIFO 182), coupled to hold the header information before it is processed by the protocol processor (Fig. 5, PPU 116), and a second FIFO buffer (Fig. 5, Output FIFO 184), coupled to receive the at least one packet header from the protocol processor (Fig. 5, PPU 116) and to deliver it to the transmit logic; regarding claim 22, wherein and the header memory comprise parallel first-in-first-out FIFO buffers (Fig. 5, Input FIFO 182, Output FIFO 184), which are arranged to hold the header portion, for a plurality of frames of incoming data; regarding claim 23, wherein the header memory comprises a first FIFO buffer (Fig. 5, Input FIFO 182), coupled to hold the header portion before it is processed by the protocol processor (Fig. 5, PPU 116), and a second FIFO buffer (Fig. 5, Output FIFO 184), coupled to receive the header information from the protocol processor (Fig. 5, PPU 116) and to deliver it to the transmit logic; regarding claim 36, wherein writing the outgoing header information comprise writing the information to parallel first-in-first-out FIFO buffers (Fig. 5, Input FIFO 182, Output FIFO 184) for a plurality of frames of outgoing data in succession; regarding claim 37, wherein processing the outgoing header information comprises writing the at least one outgoing packet header to a further FIFO buffer (Fig. 5, Output FIFO 184) in preparation for associating it with the outgoing payload data; regarding claim 46, wherein writing the header portion comprise writing

the header portion to parallel first-in-first-out FIFO buffers (Fig. 5, Input FIFO 182, Output FIFO 184) for a plurality of frames of incoming data; regarding claim 47, wherein processing the header portion comprises writing the incoming header information to a further FIFO buffer (Fig. 5, Output FIFO 184), in preparation for associating it with the incoming payload data. See column 7-11.

Bremer et al. does not disclose the following features: regarding claim 7, wherein the outgoing data memory comprise first-in-first-out FIFO buffer; regarding claim 22, the data memory comprise first-in-first-out FIFO buffer, regarding claim 36, and writing the outgoing payload data comprise writing the data to FIFO buffers for a plurality of frames; regarding claim 46, wherein writing the data portion comprise writing the data portion to FIFO buffers for a plurality of frames of incoming data. Denton et al. discloses a communication system comprising the following features: regarding claim 7, wherein the outgoing data memory comprise first-in-first-out FIFO buffer (Fig. 2, MAIN PAYLOAD FIFO 122); regarding claim 22, the data memory comprise first-in-first-out FIFO buffer (Fig. 2, MAIN PAYLOAD FIFO 122), regarding claim 36, and writing the outgoing payload data comprise writing the data to FIFO buffers (Fig. 2, MAIN PAYLOAD FIFO 122) for a plurality of frames; regarding claim 46, wherein writing the data portion comprise writing the data portion to FIFO buffers (Fig. 2, MAIN PAYLOAD FIFO 122) for a plurality of frames of incoming data. It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Bremer et al., by using the features, as taught by Denton et al., in order to provide an efficient data communication system by increasing data rate. See Denton et al., column 1, lines 5-9.

6. Claims 24 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bremer et al. (US 6,032,190) in view of Denton et al. (US 6,041,043) as applied to claims 16, 22, 40, 46 above, and further in view of Narisi et al. (US 6,810,431).

Bremer et al. and Denton et al. disclose the claimed limitations above. Bremer et al. and Denton et al. does not disclose the following features: regarding claim 24, wherein the header information comprises an instruction to the host interface logic, indicating a length of the payload data to read from the data portion in the data memory for inclusion in the incoming data frame; regarding claim 48, wherein writing the incoming header information comprises writing an instruction indicating a length of the payload data to read from the data portion in the data memory for inclusion in the incoming data frame.

Narisi et al. discloses a communication system comprising the following features: regarding claim 24, wherein the header information comprises an instruction to the host interface logic, indicating a length of the payload data (column 29, lines 50-63) to read from the data portion in the data memory for inclusion in the incoming data frame; regarding claim 48, wherein writing the incoming header information comprises writing an instruction indicating a length (column 29, lines 50-63) of the payload data to read from the data portion in the data memory for inclusion in the incoming data frame. It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Bremer et al. and Denton et al., by using the features, as taught by Narisi et al., in order to provide less costly development and optimize network performance. See Narisi et al., column 10, line 58 to column 11, line 4.

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bremer et al. (US 6,032,190) in view of Bechtolsheim et al. (US 6,343,072).

Bremer et al. discloses the claimed limitations above. Bremer et al. does not disclose the following features: regarding claim 15, comprising a shared memory, which is accessible to both the transmit and receive protocol processors via the bus. Bechtolsheim et al. discloses a communication system comprising the following features: regarding claim 15, comprising a shared memory (Fig. 1, Memory 120), which is accessible to both the transmit (Fig. 1, TX 173) and receive (Fig. 1, RX 163) protocol processors via the bus. See Abstract. It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Bremer et al., by using the features, as taught by Bechtolsheim et al., in order to provide an efficient data communication system by maximize throughput and minimize routing latency. See Bechtolsheim et al., column 1, lines 53-60.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Osborne (US 6,078,733) discloses a network interface.

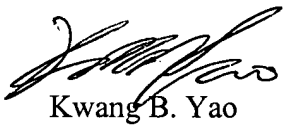
Brueckheimer et al. (US 5,917,824) discloses an ATM communications system.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kwang B. Yao whose telephone number is 571-272-3182. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KWANG BIN YAO
PRIMARY EXAMINER



Kwang B. Yao
December 1, 2004